AMENDMENTS TO THE CLAIMS

The following is a complete listing of the claims, which replaces all previous versions of the claims.

1. (currently amended) A system comprising:

a host/data controller; and

a memory system comprising a plurality of memory cartridges operably coupled to the host/data controller, each memory cartridge comprising an operation indicator configured to indicate the operational status of the corresponding memory cartridge, wherein the operation indicator comprises a bit having a first state and a second state, the first state indicating that the memory cartridge is operational and the second state indicating that the memory cartridge is not operational, wherein the memory system is configured to operate in a redundant mode when each of the bits is in the first state, wherein at least one of the host/data controller and the plurality of memory cartridges comprise error detection components, and wherein the host/data controller is configured to generate a low priority interrupt signal in response to error detection by the error detection components if each of the operation bits is in the first state.

2. (original) The system, as set forth in claim 1, wherein the memory system comprises a redundant memory system.

3. (original) The system, as set forth in claim 2, wherein the memory system comprises five memory cartridges.

4 -7. (cancelled)

8. (currently amended) The system, as set forth in claim [[6]] 1, wherein the host/data controller is configured to generate a low priority interrupt signal in response to multi-bit error detection by the error detection components if each of the operation bits is in the first state.

9. (currently amended) ~~The system, as set forth in claim 6,~~ A system comprising:

a host/data controller; and

a memory system comprising a plurality of memory cartridges operably coupled to the host/data controller, each memory cartridge comprising an operation indicator configured to indicate the operational status of the corresponding memory cartridge, wherein the operation indicator comprises a bit having a first state and a second state, the first state indicating that the memory cartridge is operational and the second state indicating that the memory cartridge is not operational, wherein the memory system is configured to operate in a redundant mode when each of the bits is in the first state, wherein at least one of the host/data controller and the plurality of memory cartridges comprise error detection components, and wherein the host/data controller is configured to generate a high priority interrupt signal in response to multi-bit error detection if at least one of the operation bits is in the second state.

10. (original) The system, as set forth in claim 1, wherein each of the plurality of memory cartridges comprises a plurality of memory devices.

11. (currently amended) A method of generating interrupts in a redundant memory, comprising the acts of:

detecting an error in a memory system;

determining the operational status of the memory system, wherein the act of determining the operational status comprises reading five operation bits, each of the operation bits indicating the operational status of a corresponding segment of the memory, the operational status comprising one of an operational state and a non-operational state; and

initiating a system interrupt signal, the type of system interrupt signal being dependent on the operational status of the memory system, wherein the act of initiating a system interrupt comprises the act of initiating a low priority system interrupt if each of the five operation bits is in the operational state.

12. (original) The method, as set forth in claim 11, wherein the act of detecting an error comprises the act of detecting a multi-bit error.

13. (original) The method, as set forth in claim 11, wherein the act of determining the operational status comprises the act of determining whether the system is operating in one of a redundant mode and a non-redundant mode.

14-16. (cancelled)

17. (currently amended) ~~The method, as set forth in claim 15~~ A method of generating interrupts in a redundant memory, comprising the acts of:

detecting an error in a memory system;

determining the operational status of the memory system, wherein the act of determining the operational status comprises reading five operation bits, each of the operation bits indicating the operational status of a corresponding segment of the memory, the operational status comprising one of an operational state and a non-operational state; and

initiating a system interrupt signal, the type of system interrupt signal being dependent on the operational status of the memory system, wherein the act of initiating a system interrupt comprises the act of initiating a high priority system interrupt if any of the five operation bits is in the non-operational state.

18-91. (cancelled)

92. (previously presented) A system comprising:

a memory cartridge comprising an operation indicator configured to indicate an operational status of the memory cartridge; and

a controller operably coupled to the memory cartridge and configured to generate a low priority interrupt if an error detection component detects a memory error and the memory cartridge is operational.

93. (previously presented) The system, as set forth in claim 92, wherein the operation indicator comprises a bit having a first state and a second state, the first state indicating that the memory cartridge is operational and the second state indicating that the memory cartridge is not operational.

94. (previously presented) The system, as set forth in claim 93, comprising a memory system comprising a plurality of the memory cartridges.

95. (previously presented) The system, as set forth in claim 94, wherein the memory system is configured to operate in a redundant mode when the bits within each of the plurality of memory cartridges are in the first state.

96. (previously presented) The system, as set forth in claim 92, wherein the controller is configured to generate a low priority interrupt signal if the error detection component detects a multi-bit error when the memory cartridge is operational.

97. (previously presented) The system, as set forth in claim 92, wherein the controller is configured to generate a high priority interrupt signal if the error detection component detects a multi-bit error when the memory cartridge is not operational.

98. (previously presented) The system, as set forth in claim 97, wherein the high priority interrupt signal comprises a non-maskable interrupt (NMI).

99. (previously presented) The system, as set forth in claim 92, wherein the controller comprises the error detection component.

100. (previously presented) The system, as set forth in claim 92, wherein the memory cartridge comprises a plurality of memory devices.

101. (previously presented) A method comprising:

detecting an error in a memory system;

determining whether the system is operating in a redundant mode or in a non-redundant mode; and

initiating a low priority system interrupt signal if the memory system is operating in the redundant mode.

102. (previously presented) The method, as set forth in claim 101, comprising initiating a high priority system interrupt if the memory system is operating in a non-redundant mode.

103. (previously presented) The method, as set forth in claim 102, wherein initiating the high priority system interrupt comprises initiating a non-maskable interrupt (NMI).

104. (previously presented) The method, as set forth in claim 101, wherein detecting the error comprises detecting a multi-bit error.

105. (previously presented) The method, as set forth in claim 101, wherein detecting an error in a memory system comprises detecting an error on a memory cartridge comprising a plurality of memory devices.

106. (previously presented) The method, as set forth in claim 101, wherein determining whether the system is operating in either a redundant mode or a non-redundant mode comprises reading a plurality of operation bits, wherein each of the operation bits indicates the operating mode of a segment of the memory system.

107. (previously presented) The method, as set forth in claim 106, wherein determining the operating mode comprises reading five operation bits.

108. (previously presented) The method, as set forth in claim 107, wherein initiating a low priority system interrupt signal comprises initiating the low priority system interrupt if each of the five operation bits is in an operational state.

109. (previously presented) The method, as set forth in claim 107, comprising initiating a high priority system interrupt if any of the five operation bits is in a non-operational state.

110-115. (canceled)

116. (new) The system, as set forth in claim 9, wherein the memory system comprises a redundant memory system.

117. (new) The system, as set forth in claim 9, wherein the memory system comprises five memory cartridges.

118. (new) The system, as set forth in claim 9, wherein each of the plurality of memory cartridges comprises a plurality of memory devices.

119. (new) The method, as set forth in claim 17, wherein the act of detecting an error comprises the act of detecting a multi-bit error.

120. (new) The method, as set forth in claim 17, wherein the act of determining the operational status comprises the act of determining whether the system is operating in one of a redundant mode and a non-redundant mode.